understood that terms, such as those defined in commonly-used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein. As used herein, expressions such as "at least one of," when preceding a list of elements, modify the entire list of elements and do not modify the individual elements of the list.

[0046] Although corresponding plan views and/or perspective views of some cross-sectional view(s) may not be shown, the cross-sectional view(s) of device structures illustrated herein provide support for a plurality of device structures that extend along two different directions as would be illustrated in a plan view, and/or in three different directions as would be illustrated in a perspective view. The two different directions may or may not be orthogonal to each other. The three different directions may include a third direction that may be orthogonal to the two different directions. The plurality of device structures may be integrated in a same electronic device. For example, when a device structure (e.g., a memory cell structure or a transistor structure) is illustrated in a cross-sectional view, an electronic device may include a plurality of the device structures (e.g., memory cell structures or transistor structures), as would be illustrated by a plan view of the electronic device. The plurality of device structures may be arranged in an array and/or in a two-dimensional pattern.

[0047] Hereinafter, an interconnection bump of a semiconductor device according to an example embodiment will be described with reference to FIG. **1**. FIG. **1** is a cross-sectional view schematically illustrating an interconnection bump of a semiconductor device according to an example embodiment.

[0048] Referring to FIG. **1**, an interconnection bump **1** of a semiconductor device according to an example embodiment may include an under bump metallurgy (UBM) layer **10**, an intermetallic compound (IMC) **20**, a solder bump **30**, and barrier layers **40**, and may further include a passivation layer **50**.

[0049] The UBM layer **10** may increase interfacial bonding strength between an electrode A of the semiconductor device and the solder bump **30**, and may also provide an electrical path. In addition, the UBM layer **10** may reduce or substantially prevent solder material from diffusing into the electrode during a reflow process. That is, an element forming the solder may be substantially prevented from permeating into the electrode A.

[0050] The UBM layer **10** may have a first surface **10***a* disposed opposite to a surface of the electrode A and in contact with the IMC **20** on an upper portion of the electrode A, and second surfaces **10***b* extending from edges of the first surface **10***a*, respectively, to be connected to the electrode A.

[0051] The first surface **10***a* may have an overall flat structure, and may define a top surface of the UBM layer **10**. The second surfaces **10***b* may have a structure slightly inclined towards the electrode A from the first surface **10***a*, and may define lateral surfaces of the UBM layer **10**.

[0052] FIG. **2** is a cross-sectional view schematically Illustrating a modified example of the aforementioned interconnection bump. As illustrated in FIG. **2**, a UBM layer **10'** may have a structure in which second surfaces **10***d* of the UBM layer **10'** extend vertically towards the electrode A from a first surface **10***c* of the UBM layer **10'**.

[0053] The UBM layer **10** may be formed of or include a metallic material electrically connected to the electrode A.

[0054] For example, the UBM layer **10** may have a multi layer structure including a titanium (Ti) layer **11** in contact with the electrode A and a nickel (Ni) layer **12** disposed on the Ti layer **11**. In addition, although not illustrated, the UBM layer **10** may have a multilayer structure including a copper (Cu) layer disposed on the Ti layer **11**, in lieu of the Ni layer **12**.

[0055] Although the example embodiment illustrates the UBM layer **10** having a multilayer structure of Ti—Ni, the type of layers to be included in the multilayer structure of the UBM layer **10** is not limited thereto. For example, the UBM layer **10** may have a multilayer structure including a chromium (Cr) layer in contact with the electrode A and a Ni layer disposed on the Cr layer, or a multilayer structure including a Cr layer and a Cu layer disposed on the Cr layer.

[0056] In addition, although the example embodiment illustrates the UBM layer **10** having a multilayer structure, the type of structure of the UBM layer **10** is not limited thereto. For example, the UBM layer **10** may have a monolayer structure formed as or including one of a Ni layer and a Cu layer.

[0057] For example, the UBM layer **10** may be formed via a sputtering process, an e-beam deposition process, or a plating process.

[0058] The IMC **20** may be formed on the first surface **10***a* of the UBM layer **10**. The IMC **20** may be formed during a reflow process in which the solder bump **30** is formed. The IMC **20** may be formed via a reaction between an element within the solder, for example, tin (Sn), and a metal in the UBM layer **10**, for example, Ni, and may form a Sn—Ni binary alloy.

[0059] The solder bump **30** may be bonded to the UBM layer **10** with the IMC **20** therebetween. That is, the solder bump **30** may be firmly bonded to the UBM layer **10** by the IMC **20** serving as a type of adhesive.

[0060] The solder bump **30** may be formed by reflowing the solder disposed on the UBM layer **10**. For example, a general alloy material such as SAC305 ($Sn_{96}5Ag_{3.0}Cu_{0.5}$) may be used as the solder.

[0061] The barrier layers **40** may cover the second surfaces **10***b* of the UBM layer **10**, respectively.

[0062] The barrier layers **40** may minimize a level of wettability thereof with respect to the solder bump **30**, and may substantially prevent the IMC **20** and the solder bump **30** from diffusing or overflowing into the second surfaces **10***b*. Such reduction or substantial prevention may be achieved by providing a material of the barrier layer **40** to have a sufficiently low level of wettability with respect to the IMC **20** and the solder bump **30**. Accordingly, the IMC **20** or the solder bump **30** may not be formed on the barrier layer **40**.

[0063] The barrier layer **40** may be an oxide layer containing at least one element of the UBM layer **10**. For example, the barrier layer **40** may be an oxide layer containing at least one of Ni and Cu.

[0064] The barrier layers **40** may be formed by oxidizing the second surfaces **10***b* of the UBM layer **10**, and for example, may be formed by oxidizing the second surfaces **10***b* of the UBM layer **10** by performing a thermal oxidation process or a plasma oxidation process.

[0065] The passivation layer **50** may be disposed adjacently to the UBM layer **10** on the electrode A. For example,